

Polish electronics in high energy physics and aerospace technology

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Abstract—The Department of Microelectronics and Computer Science of the Lodz University of Technology possesses considerable expertise in the field of designing electronic and microelectronic systems for a wide range of applications. DMCS design teams have participated in a large number of national and international scientific research programs, grants and commercial contracts. Many of these projects have resulted in introducing new systems in scientific installations or launching new commercial products on the open market. The paper presents selected works focused on research aspects concerning accelerator control systems for high energy physics, nuclear fusion based new energy sources and design of integrated electronics for space applications.

The Department of Microelectronics and Computer Science (Lodz University of Technology) started its scientific collaboration with Deutsches Elektronen-Synchrotron (DESY) in 2002.

Since that time both parties have been cooperating in multiple areas concerning subsystems of Free Electron Laser (FEL) facilities. The main focus of these works are FEL projects located in DESY. Both Free Electron Laser in Hamburg (FLASH) and European X-ray Free Electron Lasers (European X-FEL) are located in Hamburg. The aforementioned facilities consist of linear accelerators built in TESLA [1] technology.

This technology, initially developed by DESY, defines the niobium cavity as a fundamental component for electron beam acceleration. TESLA resonators are superconducting structures crafted for particles acceleration in an electro-magnetic field (with a frequency of 1,3GHz). The standing wave generated in these tubes transfers energy to electron bunches (generated in the RF-gun) causing beam energy to increase during its way along the linac (linear particle accelerator).

Optimal beam acceleration requires precise control of field parameters (as for XFEL: an amplitude stability of 0.01dA/A and a phase stability of 0.01deg). This requirement can be met thanks to the application of a Low Level Radio Frequency (LLRF) control system.

The LLRF is a digital electronic system which utilizes a fast feedback algorithm. Its main goal is the minimization of errors between the desired field and the one measured in the superconducting structures.

During a long time of cooperation, several scientists from DMCS have been involved in the design, development, implementation and evaluation of fundamental LLRF system components. They have been actively involved in hardware systems (including a patented radiation detector [2]), firmware and software related activities.

Starting from 2003, DMCS has participated in creating the main system hardware components.

The work began with the LLRF controller design based on an FPGA chip (designed in the VME standard [3]). The latest solutions of this part are based on the MTCA standard [4]. The evaluation phase and mass production for X-FEL purposes are taking place in Lodz, Warsaw and Hamburg.

Over the years, the DMCS team members have co-designed and evaluated hardware modules for precise tuning of mechanical cavity subsystems. The system (based on piezoelectric stacks) provides fine cavity tuning in the presence of high accelerating fields (the gradient higher than 20MV/m) [5]. In the case of resonator operation in such conditions, high Lorentz force causes the walls deformation of the cavity and its further detuning from the base frequency.

Among many activities that involved work on software, the DMCS team members were co-authors of:

- firmware for fast feedback loop algorithm realization,
- system drivers for hardware components access,
- main server for LLRF system configuration, management and operation,
- server for diagnostics of the LLRF parameters,
- several slow feedbacks required for system availability maximization,
- software for examination of the cavities and cryogenics modules (for newly produced X-FEL modules),
- servers for optical synchronization subsystem for the linac.

As the global energy consumption increases, the provision of efficient and clean energy becomes an urgent necessity. One of the most promising ways of energy production is the use of nuclear fusion in thermonuclear

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reactors, such as tokamaks, in which plasma is magnetically confined in a toroidal shape.

The Lodz University of Technology is also involved in the design of the world's largest thermonuclear reactor called ITER. ITER is a large-scale scientific experiment conducted together by researchers from the European Union, India, Japan, Korea, Russia, China and the United States. It is built on the experience gained from the latest experiments, like Joint European Torus (JET) and Tore Supra. It will be the most technologically advanced tokamak so far. It is assumed to be able to produce 500 MW of energy with an efficiency coefficient of 10. The machine is now being constructed at ITER, a non-profit scientific institution in Cadarache, France. As the site construction process progresses, the need for developing a sophisticated control and monitoring system is emerging. Being the result of the ITER project, the technology will be able to be commercialized in 2050, but the tokamak assembly should start in 2018 and by then the concept for its instrumentation should be finished. Building and operating the machine requires multidisciplinary effort not only by physicists but also by engineers.

Poland's scientific contribution to the project is currently limited to physicists involved in plasma experiments. Polish scientists are missing the unique opportunity to gain experience in the area of technology and engineering. It is crucial for Poland to get involved in the technological aspects of the experiment and create an international network of competence. Since the EU tends to reduce CO₂ emissions, a new technology of energy production is especially crucial for Poland.

The Lodz University of Technology is responsible for the design, development and testing of data acquisition systems. The data acquisition systems are built using various platforms: Advanced Telecommunications Computing Architecture (ATCA), MicroTelecommunications Computing Architecture (MicroTCA), and PCIe eXtensions for Instrumentation (PXIe). The big advantage of xTCA (MicroTCA and ATCA) systems is embedded health monitoring and advanced management based on an Intelligent Platform Management Interface (IPMI) [5-7].

The Image Acquisition System (IAS) was designed using the MicroTCA.4 standard [8]. The system is dedicated to operating with high-resolution fast cameras equipped with a Camera Link interface. The image data provided by a digital camera are received by a frame grabber card and transmitted to the host via a PCIe interface. The modular structure of the MicroTCA.4 architecture allows connecting various cameras to a single MTCA chassis. The system supports nanosecond synchronization with time reference using the IEEE1588 Precision Time Protocol [9].

The data from the digital cameras are transferred to the frame grabber module, built as an Advanced Mezzanine

Card (AMC). The MicroTCA chassis is connected to an external CPU blade via a PCIe cable. Using high-performance DMA bulk transfers, the image data from the frame grabber card are transferred directly to the host computer memory. The received data are further processed and sent next via a 10Gb Ethernet network for archiving and machine control. Low level firmware was developed for Xilinx Virtex 5 FPGA. The high level software support for the IAS includes low-level Linux drivers, libraries for all components and high-level EPICS-based environment for system control and monitoring.

The Neutron Flux Measurement (NFM) prototype was developed using NI PXIe hardware. The system measures the total emission of neutrons from plasma and therefore allows calculating fusion power and its evolution in the time domain. The analog signal from the neutron detector is connected to a fast digitizer module. The pulsed signal is first digitized and then forwarded to a fast real-time data processing unit that operates in the required mode. In the PXIe-based NFM Plant I&C implementation, the signals from the fission chambers are acquired by a four-channel ADC module NI 5761R attached to FlexRIO PXIe-7966R located in the NI PXIe-1065 chassis. The NI PXI-6683H timing module ensures synchronization of the system to the ITER time using TCN. The PXIe chassis is connected via the PCI Express link to the ITER fast controller CPU running CODAC Core System [10], applied to acquire, process, archive and display measured neutron parameters.

DMCS has been involved in an ASIC project intended for operation in open space conditions, including radiation. DMCS is one of the contractors working in a consortium founded specially to design an integrated circuit that has been proposed to and accepted by the European Space Agency (ESA).

The consortium members are also: Astri Polska z o. o. company (a daughter-company of the Airbus Space and Defence – former Astrium), Space Research Center of the Polish Academy of Sciences and Integrated Systems Development S.A. (ISD) from Greece. The role of DMCS is to co-design the ASIC [11] along with Astri Polska.

The main property of the systems for space applications is the ability to operate without any maintenance, which in the case of satellites can mean dozens of years. So far, many electronic components and systems have been designed in a classic way, as PCB-based circuits. Although this is a well-grounded approach, it has the following drawbacks:

- sensitivity to space environment: passive and active analog elements change their parameters over time due to harsh environmental influence [12];
- damage caused by high energetic particles, e.g. Single Event Effects (SEE) [13];

- Time-consuming and expensive design due to a huge number of discrete electronic components [14]. Compared to discrete electronics, the ASIC approach provides several improvements:
- additional process/design steps that improve resistance to TID, SEE and Single Event Latch-up (SEL);
- lower number of system components, which means more uniform environmental impact on the system [15];
- reduction of dimensions, mass and power requirements.

The designed ASIC is a DC/DC converter controller [11]. It is the environmental issues that make the circuit design a far more untypical and demanding process. One of them is rad-hardness of the final circuit. If a typical CMOS technology process is utilized, there is a need for design and qualification of rad-hard component libraries. This is a long and expensive process (rad-hardness by design). The consortium has chosen another way by selecting Silicon on the Insulator (SoI) process.

The DC/DC converter under design is an analog ASIC, though several mixed-signal and digital approaches were discussed with ESA and may be the focus of future work. The most crucial sub-circuits of the designed converter are: a voltage error amplifier, current error amplifiers, PWM comparator, voltage reference, output stage driver. The designed DC/DC converter ASIC should work in the voltage- and current-based control modes. Also, the cooperation of two converters should be possible, so that a complex scheme of DC/DC voltage conversion can be realized without necessitating a new hardware application.

The task of the project is to provide a space application ready circuit. The design of ASIC will be finished by a specialized space qualification process, and this is where the Space Research Center has very much experience.

The achievements presented in this paper clearly show DMCS's long-term and in-depth involvement in research related to the design of electronic systems intended for operating in harsh conditions. The achievements in such fields show considerable expertise of DMCS teams.

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