

## Digital techniques for noise reduction in CCD detectors

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**Abstract**— Charge Coupled Devices (CCDs) have been recently commonly used in many advanced scientific and industrial research projects. They became especially popular in astronomy observations like the “*Pi of the Sky*” experiment. This paper describes the hardware being developed for the needs of this experiment to allow applying certain digital readout and noise reduction techniques developed for ultra-sensitive CCD detectors.

### Innovative methodology for sky observations

The “*Pi of the Sky*” experiment was initiated by the Soltan Institute for Nuclear Studies in Warsaw to search for dynamic optical objects. Its main goal is the detection of Gamma Ray Bursts (GRBs) counterparts in the optical spectrum. Considering their isotropic distribution all over the sky and the time period of gamma radiation varying between milliseconds and minutes, a dedicated observation system was designed which consists of 32 cameras, 2048x2048 pixels each, working in parallel and covering a large part of the sky [2].

The hardware of the cameras mentioned is divided into two parts: analogue and digital which are assembled on separate boards. Hence the sensitive analogue signal chain including a CCD device together with a dedicated video processor AD9826 was easily and efficiently separated from digital interferences. This system implements the classical technique of a video signal readout referred to as Correlated Double Sampling (CDS). The CDS module is followed by 16 bit ADC. The noise achieved in the described cameras is less than  $12e^-$  at 1MHz readout speed and less than  $16e^-$  at 2MHz. Such parameters are satisfactory for 10 seconds of exposure time.

New requirements for a sky observation system specify much shorter integration periods. In order to preserve the detector range, the readout noise needs to be reduced significantly [1].

### Alternative video signal processing techniques for CCD detectors

CCD's output signal for a given pixel is composed of two interesting levels referred to as reference level (i.e. dark level) and pixel level. The information of light intensity in the pixel's area is hidden in the difference of those levels. A CDS operation means simply capturing a

sample of each level and then subtracting them with a differential amplifier.

Although this technique is commonly used because of its simplicity, there has been certain different readout techniques developed resulting in better noise performance of the signal processing chain. They are based on elaboration of filters optimized for increasing the system's SNR.

The first of them, referred to as *Zero Noise CCD*, was designed at French and German observatories. It is based on analog-to-digital conversion of a video signal directly after the detector's output and its further digital processing. Additionally, video signal oversampling was used (with sampling frequency much higher than the pixel rate) resulting in a set of samples relating to each pixel. Such a system minimizes the amount of noise sources by limiting analogue modules to the minimum and creates an opportunity to elaborate a filtration algorithm resulting in the best SNR performance.

The simulation of a CDS processor carried out in this system resulted in a noise of  $3.1e^-$  with the internal noise of the detector used of  $3.0e^-$ . This has proven the minimum noise introduced by the system itself. Further research on filters with the Gaussian distribution of coefficients led to noise reduction to a level of  $2.2e^-$ . Finally, after optimization of the coefficients with a simulated annealing algorithm, the noise level of  $1.7e^-$  was achieved in the system, where the CDS technique gained only  $5e^-$ .

Another interesting technique is dual slope integration which (provided that the dominant noise component in the signal is white) is equivalent to optimal filtration in terms of SNR. Such an assumption is usually met for CCDs at high readout speeds [4]-[5]. Dual slope integration in a digital domain means (assuming there are a number of signal samples available for each pixel) computing mean values for the reference and pixel levels and subtracting them. Knowing that the variance (i.e. power) of white noise falls down with the square root of the number of samples used, it is obvious that such an operation increases the noise performance of the system.

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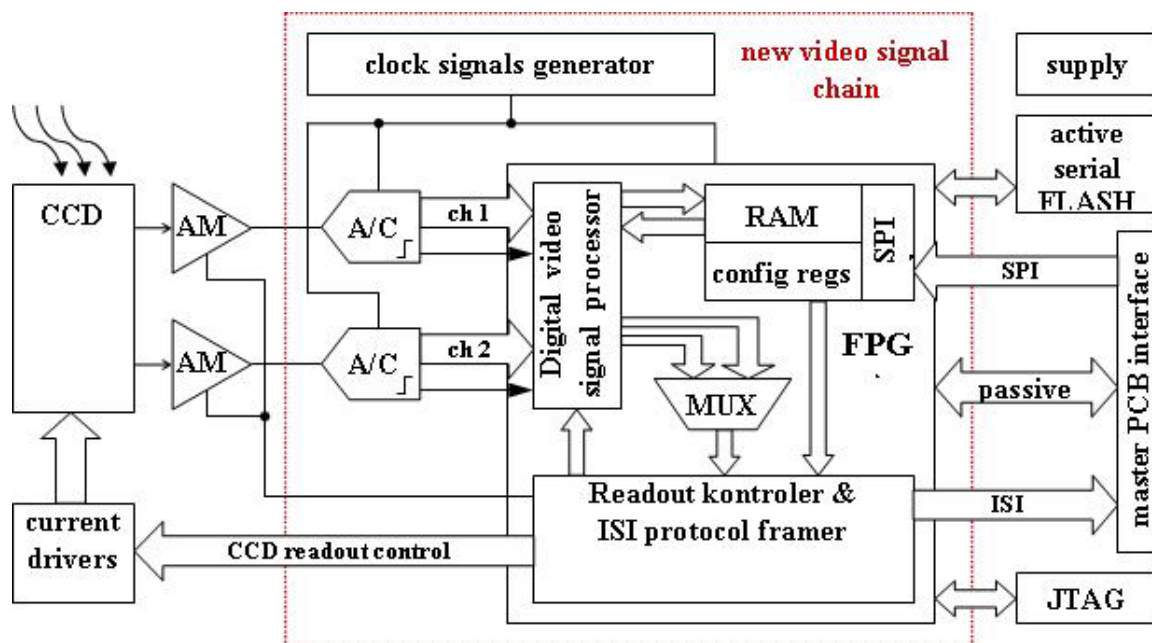


Fig. 1: Block diagram of a circuit enabling digital video signal processing for CCD image sensors

The implementation of readout techniques like those described above should result in increased SNR compared to CDS. Hoping for an opportunity to preserve current noise performance of “*Pi of the Sky*” cameras at higher pixel rates and lower exposure times, a system allowing for digital signal processing of CCD’s output signal was designed.

### Hardware design

The prototype system was based on the newest K30 “*Pi of the Sky*” cameras. Taking into consideration high prices of CCD chips the prototype is equipped with, an FA2048 detector from Loral Company is used in the experimental design. The final system is going to be equipped with a much newer STA0820 detector. To achieve the simplicity of design and provide reliable synchronization between various functional modules (analog to digital converters, video signal processor, and CCD readout controller), the signal processor and readout drivers were realized in one circuit clocked with the same signal as ADCs. The whole circuit was placed on the PCB with an image detector. A block diagram of the system realizing such a concept is shown in Fig. 1 and the assembled PCB - in Fig. 2.

This way analog to digital converters became the first (just after DC restoration and initial amplification) stage of a video signal processing chain. Achieving high signal oversampling with the pixel rates usually present in “*Pi of the Sky*” experiment cameras (varying from hundreds of kHz up to 2MHz) required the usage of ADCs working with a sampling rate of the order of tens to hundreds of MHz.

Preserving the optical range of the system, on the other hand, required conversion with at least 12 effective bits. Finally, from the range of elements available on the market an LTC2209 converter was chosen with a sampling frequency up to 160MSPS and Effective Number of Bits (ENOB) of almost 13 bits (76.7dB). To utilize its performance an ultra-low-jitter clock generator was needed. A MAX3624 circuit was used which provides the jitter of 360fs among with a simple configuration schedule.

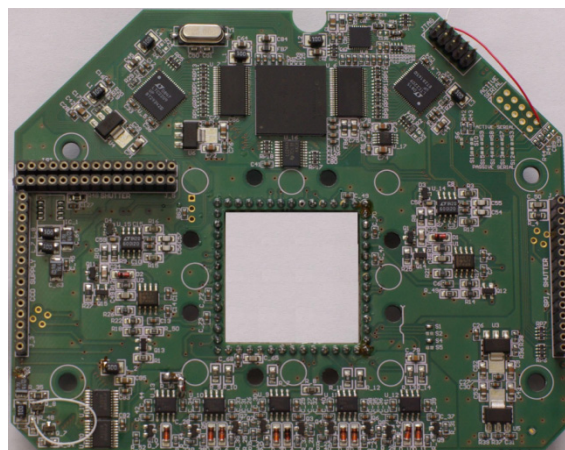


Fig. 2. PCB with a digital CCD video signal readout assembled for “*Pi of the Sky*” cameras.

To provide efficient synchronization of the overall readout operation a new video signal processor was integrated with a CCD readout controller. Both these functions are performed by an FPGA device from the Cyclone III family. It communicates with the master

camera board for a readout configuration and setup through an SPI serial interface bus.

The data produced by the video signal processor are formed into frames compatible with the Image Sensor Interface (ISI) of the main camera processor.

The functionality of the system designed was initially verified in laboratory environment. Altera's Signal Tap Analyser was used to capture the signals inside the FPGA device. The results are shown in Fig. 3, where consecutive video signal levels for one pixel are visible. The test was provided with a pixel rate of 1MHz and ADC's sampling rate of 150MSPS resulting in about a hundred useful samples of the video signal for each pixel.

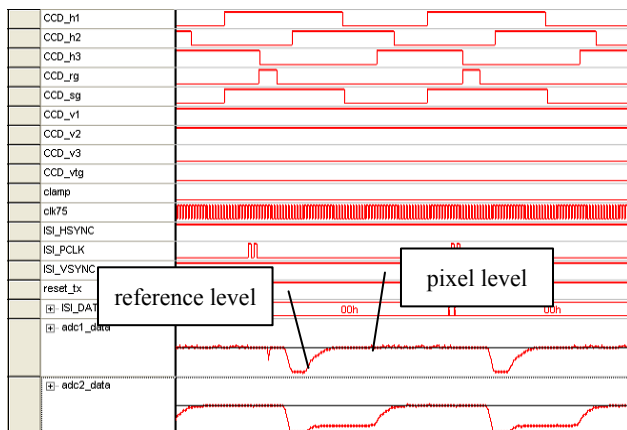


Fig. 3. Samples of CCD video signal inside FPGA device as a result of real time analysis.

### Summary and further development perspectives

The tests provided and proved proper operation of the designed circuitry with a CCD detector. High oversampling of the video signal resulted in a large amount of samples related to each pixel and allows to elaborate and compare various digital signal processing techniques. The device can be used as an environment to implement and test them.

However, applying such a system in the current design of "Pi of the Sky" cameras has one significant disadvantage – we were forced to place ADCs near the detector. Their high power consumption produces a significant amount of power that leads to noticeable distribution of heat on the PCB whereas CCDs require low temperatures for low noise operation. Provided that initial results are promising, the whole camera mechanics will be redesigned to meet new cooling requirements.

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