Tradeoff between mode confinement, loss, and cross-talk, for dielectric and metal slot waveguides

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Abstract— Slot waveguides formed in high-index dielectrics or metals provide strong field enhancement in the slot region. When filled with nonlinear or lasing materials, they have the potential for highly efficient components for intensity dependent signal processing in integrated photonic circuits. In view of the increasing demand for high integration, metal slot waveguides have the great advantage of sub-diffraction mode confinement but they suffer from serious transmission loss. The total lateral field extent in their low-loss dielectric counterparts is, in turn, diffraction limited. Considering those tradeoffs, we show that at 24dB/μm cross-talk and the attenuation length of at least 5μm, gold slot waveguides can be spaced only ca 3.5 times denser than slot waveguides in silicon.

Slot waveguides made in a high index contrast dielectric, which are capable of sub-wavelength light localization in the slot region [1] are considered to be attractive potential components for the enhancement of amplification or signal processing functions relying on nonlinear effects. However, their feasibility for use in densely integrated photonic circuits is limited by the fact that the total lateral field extent still obeys the diffraction limit.

When a slot waveguide is formed in metal [2], the total lateral field can be shrunk far beyond the diffraction limit, which implies that metal (plasmon) slot waveguides can be much more densely spaced. It is often claimed that with plasmon waveguides the integration density can be increased by orders of magnitude. Unfortunately, due to intrinsically high optical absorption in the metal walls the propagation loss is 3 - 4 orders of magnitudes larger than in dielectric waveguides and in addition, strongly increases with a decreasing size of the slot. This is likely to diminish the integration advantage of a plasmon slot waveguide over its diffraction-limited dielectric counterpart. To see how large this advantage can still be we compare attainable packing densities for straight 3D plasmon and silicon (Si) slot waveguides at a predefined maximum level of propagation loss (or the corresponding attenuation length). As a measure of packing density we use center-to-center separation (pitch) between an identical a pair of parallel waveguides at a given level of cross-talk. We express cross-talk in terms of a coupling length determined from beating between the lowest-order supermodes [3 and refs. in there] of a directional coupler. Effective indices of the supermodes are calculated using the COMSOL mode solver.

The maximum admissible propagation loss determines not only how narrow the plasmon waveguide can be, but also how tightly the edges of two waveguides can be separated. This is because in the strong coupling regime larger power fraction of the symmetric supermode is carried by the metal separating two slots, and hence the propagation loss is larger than for well separated, weakly coupled waveguides [3]. Taking this into account, as well as the theoretical loss values for an isolated slot waveguide in gold [1], we set the limit of 100nm on the minimum slot width in order to obtain the attenuation length of at least 5μm. Although this constraint is not applicable to a slot in Si, we keep the slot widths equal while comparing the packing densities. As a reference we also consider Si photonic wire that provides the highest integration density among the diffraction limited waveguides [4]. For each of the three waveguide types we have made some parameter optimization starting from the published results or guidelines relevant to the particular cases [4, 5, 6].

We consider two parallel plasmon and Si slot waveguides with the cross sections shown in Fig. 1 and Fig. 2, respectively.

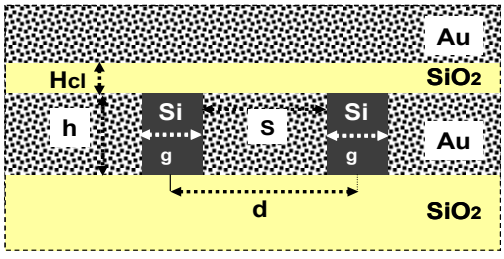

Fig. 1. Cross section of two parallel plasmon slot waveguides.

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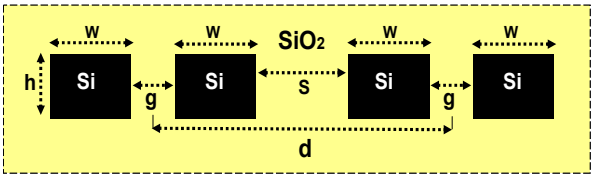

Fig. 2. Cross section of two parallel Si slot waveguides.

The reference Si wire is a Si channel waveguide surrounded by SiO2 cladding. The thickness of all the waveguides is h=250nm. For the assessment of the packing density we analyze the coupling between two identical parallel waveguides. The analysis is made assuming the acceptable coupling length Lc=25μm, which corresponds to ca 24dB/μm crosstalk.

Fig. 3 and Fig. 4 show how the pitch for the respective slot waveguides varies with the slot width g at the fixed value of Lc=25μm indicated by the dashed line. For a Si slot waveguide we have also optimized the width W of the

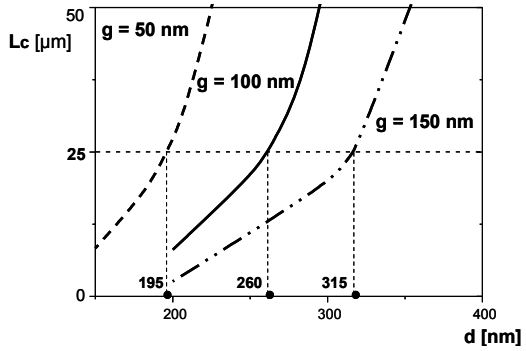

Fig. 3. Coupling length vs pitch d for the plasmon slot waveguide coupler, and for different values of the slot width g: 50nm, 100nm, 150nm.

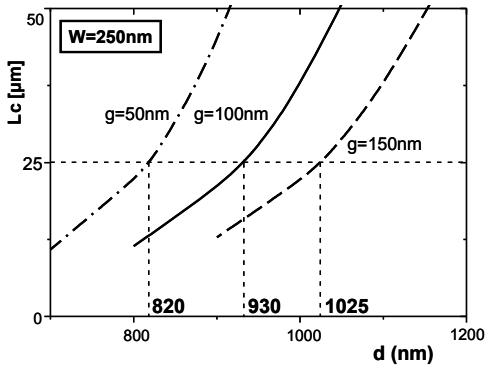

Fig. 4. Coupling length vs pitch d for a Si slot waveguide coupler, and for different values of the slot width g: 50nm, 100nm, 150nm. The width of the cladding for Si slot waveguide is W=250nm.

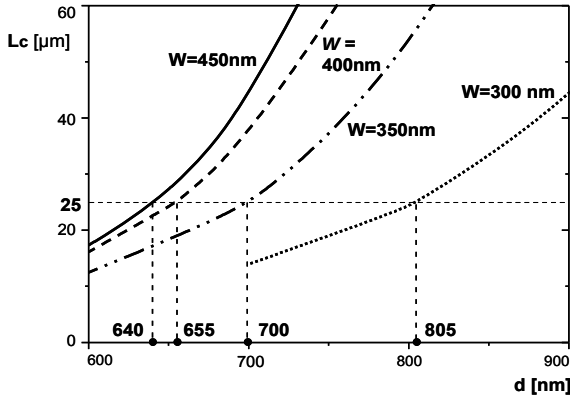

Fig. 5. Coupling length vs pitch d for the Si wire coupler for different values of the core width W: 300nm, 350nm, 400nm, 450nm.

silicon cladding. The curves shown in Fig. 4 are obtained for W=250nm, which gives the smallest pitch values at Lc=25μm.

Fig. 5 illustrates how the pitch for the Si wire waveguides varies with the core width W for Lc=25μm (dashed line).

For slot waveguides the packing density clearly increases with a decreasing core (slot) width since the field becomes stronger confined in the slot. However, below a certain value of the edge-to-edge separation, which is much larger for the Si slot waveguides, strong waveguide coupling will dominate the effect of the slot narrowing. In addition, the need of sufficiently wide silicon cladding further limits the integration density.

For photonic wires a decrease in the core width below a certain value (ca 450nm for the considered Si wire) results in widening of the modal field, hence the packing density decreases. More detailed analysis for dielectric slot and wire waveguides, where also comparison of the bending loss is included, can be found in [4].

Here we focus on comparing the packing densities for the considered plasmon and Si slot waveguides subject to the condition that the minimum attenuation length is at least 5μm. Using the theoretical propagation loss values for the plasmon slot waveguide of Ref. [2], and considering the excesses loss in the strong coupling regime [3], we conclude that the loss requirement is satisfied for the slot widths starting from ca 100nm and larger. To keep field confinement similar we compare the plasmon and Si slot waveguides of the same slot width. The results, where also Si wire is included as a reference, are shown in Fig. 6.

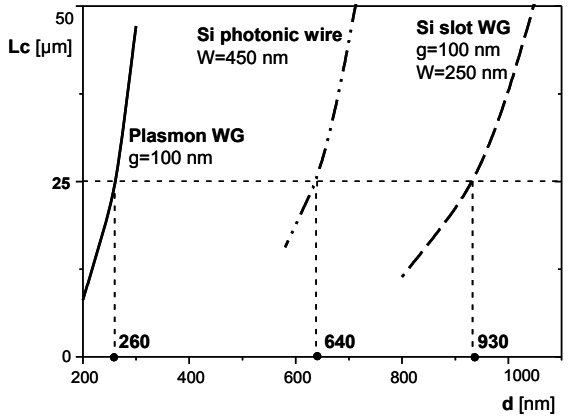

Fig. 6. Coupling length vs pitch d for the considered waveguide types: plasmon slot waveguide, Si wire, and Si slot waguide. Note that W for Si wire is a core width, while for Si slot waveguide it stands for the Si cladding width. g is the width of a slot.

Comparing the values of the pitch for Lc=25, we find that the pitch, hence the packing density, of the plasmon slot waveguide is 3.57 times smaller than the pitch of the Si slot waveguide, and 2.46 smaller than that for the Si wire. Would one resign from the comparable field confinement and use 50nm wide Si slot for the comparison, the pitch of the plasmon slot waveguide would be 3.15 times smaller, which does not make a big difference. The packing density obtained for the plasmon slot waveguide is significantly, but not dramatically larger than that of the Si slot waveguide, whereas the losses are 3 – 4 orders of magnitude larger. Unfortunately, the loss drawback overrides the integration density benefits and hinders the use of plasmon slot waveguides for large scale integration. However, while integrated with low-loss Si wire or a Si slot waveguide, they may possibly be used as part of the device.

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