Low-Cost Precision Patterning of Transparent Conductors and Failure Mode Analysis for Liquid Crystal Meandered Delay Lines

Jinfeng Li*[1,2,3]

[1]*School of Interdisciplinary Science, Beijing Institute of Technology, Beijing, 100081, China,*
[2]*Beijing Key Laboratory of Millimeter Wave and Terahertz, Beijing Institute of Technology, Beijing, 100081, China,*
[3]*Electrical and Electronic Engineering Department, Imperial College London, London SW7 2AZ, United Kingdom*

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Abstract—This letter details an optimized, low-cost process for the photolithographic patterning of Indium Tin Oxide (ITO) on glass and polycarbonate (PC) substrates for applications in microwave devices, such as liquid crystal-embedded meandered delay lines. A comprehensive fabrication protocol for both substrate types is presented, utilizing positive photoresists (AZ4562 and AZ5214E) and hydrochloric acid (HCl) etching. While high-fidelity patterning with sub-micron accuracy was achieved on glass substrates, the implementation on PC substrates revealed a critical failure mode: film cracking induced by thermal expansion coefficient mismatch. This study investigates the root cause of this cracking, linking it to the significant difference in the Coefficients of Thermal Expansion (CTE) between ITO ($8.5 \cdot 10^{-6}$ /K) and PC ($70.2 \cdot 10^{-6}$ /K). We demonstrate that replacing conventional thermal processing with room-temperature dehydration in a vacuum desiccator successfully mitigates this failure, enabling the fabrication of uniform and accurate ITO patterns on thermally sensitive polymer substrates.

Transparent conductive oxides, particularly Indium Tin Oxide (ITO), are critical components in a wide range of optoelectronic and microwave devices due to their excellent combination of electrical conductivity and optical transparency [1−2]. One emerging application is in tunable liquid crystal (LC) based phase shifters and delay lines [3] for microwave (MW) systems [4], where ITO electrodes are used to apply electric fields to the LC layer. The performance of these devices is highly dependent on the precision and integrity of the patterned ITO electrodes.

While silicon and glass are common substrates, there is a growing interest in using polymers like polycarbonate (PC) for their advantages in weight, cost, flexibility, and impact resistance. However, the fabrication of high-quality ITO films on polymer substrates presents significant challenges, primarily due to the low glass transition temperature and high thermal expansion coefficient of polymers compared to inorganic materials like ITO. To this end, this work presents a comprehensive study on a low-cost photolithography and wet-etch process for patterning ITO for LC-embedded meandered MW delay lines (width of 210 μm for 50 Ω impedance matching), as illustrated in Fig. 1 for the mask and the post-etch patterns (prior to stripping the AZ4562 photoresist).

* jinfengcambridge@bit.edu.cn

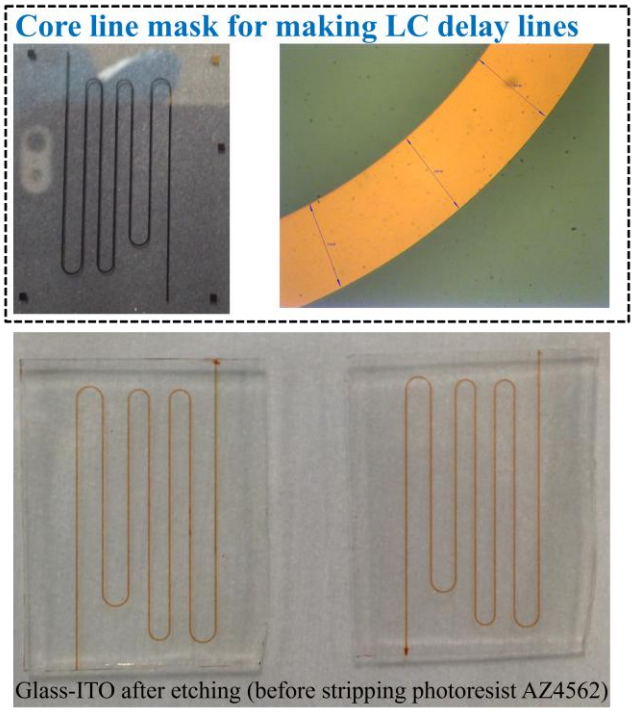

Fig. 1. Key manufacturing process of glass-ITO photolithography for LC-embedded meandered transparent microstrip delay lines (targeting 0-360° reconfigurable differential phase shifts).

We first establish a reliable and detailed protocol for patterning ITO on glass, achieving feature resolutions below 1 μm (Fig. 1). Subsequently, we transition this process to PC substrates and identify a predominant failure mode: micro-cracking of the ITO film. A systematic failure mode analysis is conducted, pinpointing thermal stress during processing as the root cause. Finally, we propose and validate a low-thermal-budget processing strategy that eliminates cracking and enables the successful fabrication of ITO patterns on PC for advanced microwave devices. The substrates used were 35 mm×28 mm ITO-coated glass sheets (sheet resistance ~120 Ω/□). Failed patterns could be stripped using acetone, allowing

for substrate reuse. The cleaning procedure was critical: substrates were sonicated in acetone to remove organic contaminants, followed by isopropanol (IPA) sonication and a deionized (DI) water rinse. Drying was performed with a N_2 gun (can introduce contaminants if not filtered); using a hotplate for drying is a viable alternative. Two photoresists were attempted, i.e., AZ4562 (thick film) and AZ5214E (thin film). For AZ4562 spin-coated at 4000 rpm for 30s, a soft bake was performed at 90°C for 1 min, followed by a 10-min rehydration period at ambient conditions. UV exposure was performed using a high-pressure mercury lamp (wavelength: 365 nm, intensity: ~15 mW/cm² measured at the sample surface). Development was carried out in AZ351B developer diluted 1:3 with DI water for 5 min. For AZ5214E spin-coated at 4000 rpm for 30s, soft bake was at 90°C (1 min), followed by a 1-min rehydration. UV exposure was reduced to 3s. Development in AZ351B (1:4 dilution) was closely monitored; endpoint was determined by disappearance of thin-film interference fringes (<1 min). After development, both processes included a DI water rinse, acetone edge-bead removal, a final DI rinse, and inspection under a microscope. A hard bake (115°C for AZ4562, 120°C for AZ5214E) was performed for 2 min to strengthen the resist prior to etching. Etching was performed in a 25% Hydrochloric Acid (HCl) solution maintained at 50−60°C for 2 min. This temperature was found to provide optimal surface roughness. Safety protocols were followed when handling and diluting concentrated acids, always adding acid to water to mitigate violent exothermic reactions. After etching, the substrates were immersed in DI water to halt the process. The photoresist mask was finally stripped using acetone, followed by a DI water rinse and drying. Established process on glass substrates yielded excellent results. Post-etching inspection before resist stripping confirmed horizontal patterning errors of < 1 μm (Fig. 1). Electrical characterization of the patterned ITO lines showed low resistance, measuring 70 Ω and 7 Ω for two different samples, verifying integrity of the conductive pathways.

The process was modified for ITO-coated PC due to its thermal sensitivity. Acetone, a potent solvent for PC, was replaced in the cleaning and stripping steps. Ethanol (96%) was used for cleaning, and a mild KOH solution was used for photoresist stripping. The most critical modification involved the thermal budget. Initial attempts to use a standard soft bake at 50°C for 10 min failed, resulting in poor feature definition. More severely, standard hard bake temperatures ($\geqslant$115°C) consistently led to widespread cracking of the ITO film, as shown in Fig. 2. The primary failure mode observed on PC substrates was the cracking and delamination of the ITO film. This failure is attributed directly to the mismatch in the Coefficients of Thermal Expansion (CTE) between the ITO film (CTE ~ 8.5×10^{-6}/K) and the PC substrate (CTE ~ 70.2×10^{-6}/K), nearly an order of magnitude difference. For comparison, the CTE of glass is approximately $3.2–9.0 \times 10^{-6}$ /K, which is well-matched to ITO. During the hard bake at 115°C, both materials (ITO and PC) expand. Due to its much higher CTE, the PC substrate expands significantly more than the brittle ITO film. Upon cooling, the PC substrate contracts more rapidly and to a greater extent than the ITO. The ITO film, being stiff and brittle, cannot accommodate this large compressive strain from the contracting substrate. This generates high internal tensile stress within the ITO, which is relieved through the formation and propagation of micro-cracks, as illustrated in Fig. 2 (post baked, exposed and developed). These cracks propagate throughout the film, leading to a loss of electrical conductivity and structural integrity (as illustrated in Fig. 3).

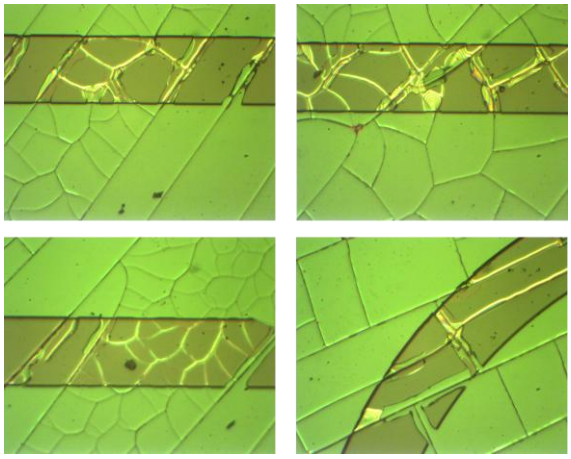

Fig. 2: Optical micrographs showing extensive cracking networks in ITO film on PC substrate after a standard 115°C hard bake process.

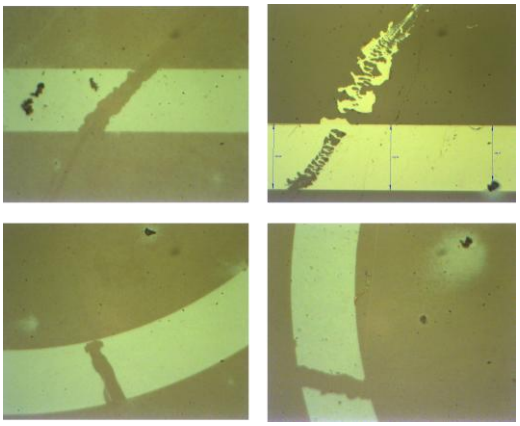

Fig. 3: Crack-related failure modes of the LC meandered delay line.

To mitigate this thermally induced failure (open circuits, contaminations, parasitic coupling effects, impedance

mismatch, etc.), the thermal budget of the process was radically reduced. The conventional thermal soft bake and hard bake steps were eliminated for the PC substrate process. After spin-coating the photoresist, the PC substrate was placed in a vacuum desiccator at room temperature for an afternoon to facilitate dehydration. Subsequently, the substrate was left in ambient air for one week to allow for complete solvent evaporation and resist stabilization through rehydration.

This process, while longer, subjects the substrate to no elevated temperatures. This low-thermal-budget approach successfully eliminated the cracking failure modes occurred in Fig 3. The resulting ITO patterns on PC were demonstrated to be uniform and accurate, with features matching the mask design (as photographed in the top images of Fig. 1). The PC etching process proceeded successfully without film damage, confirming that the primary cause of failure was the thermal stress from baking, not chemical or mechanical effects during other procedural steps.

As photographed and characterized in Fig. 4 below, a comparison of the failed (left column) and successful (right column) PC substrates is evidenced for the experimented LC-embedded tunable delay lines (for feeding X band phased array antenna applications targeting space communications and radio instrumentation [4]) in a compact meandered inverted microstrip line (IMSL) configuration [5], wherein the core line's patterns are formulated from the ITO film coated on the PC substrate.

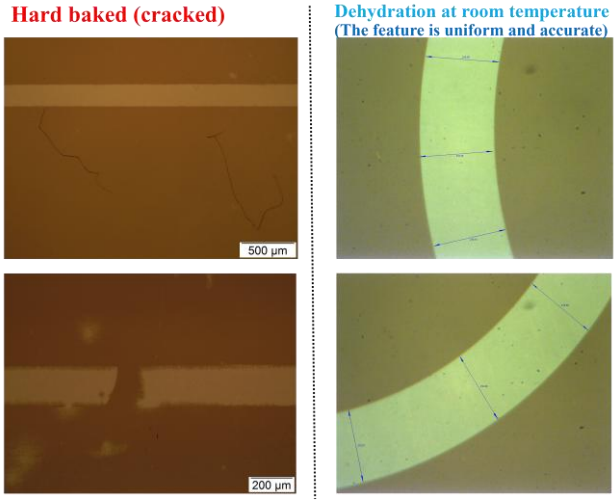

Fig. 4: Comparison of cracked ITO patterns on PC from a high-temperature hard bake process (left column) vs. a uniform, crack-free ITO pattern on PC achieved using a proposed room-temperature vacuum desiccation process (right column).

In the top-left image, micro-cracks initiate at the ITO line edges and propagate outward into the surrounding film. These edge-initiated cracks indicate stress concentration at pattern boundaries and precede complete line failure.

In conclusion, this letter has presented a detailed low-cost (clean-room-free) methodology for the precision patterning of ITO on both glass and polycarbonate (PC) substrates. The process on glass is robust and yields high-fidelity patterns with sub-micron accuracy. The transfer of this process to polycarbonate revealed a critical failure mode—cracking of the ITO film—driven by the significant mismatch in thermal expansion coefficients (CTE). The CTE of ITO is roughly an order of magnitude lower than that of the polymers. Through systematic experimentation and comparative analysis, we identified the hard bake step as the root cause of the failure. We successfully developed and validated a mitigation strategy that replaces all high-temperature steps with a prolonged room-temperature dehydration process in a vacuum desiccator. This solution enables the reliable fabrication of ITO patterns on thermally sensitive PC substrates. This advancement is crucial for developing transparent, low-cost, and robust LC-enabled MW delay lines [6–8] and other polymer-based electronic devices [9–11].

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